NVIDIA Jetson Xavier NX Pin and Function Names Guide

Application Note

DA-10009-001_v1.0 | June 2020

Document History

DA-10009-001_v1.0

Version	Date	Description of Change
1.0	June 11, 2020	Initial Release

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Introduction

The NVIDIA® Jetson Xavier NX™ series System on Module (SOM) is built around the NVIDIA® Xavier™ System on Chip (SoC). Jetson Xavier NX documentation often refers to names of interfaces, pins, functions, etc., from a SOM perspective. However, other documentation (for example, the TRM) will necessarily take a SoC perspective. Some documentation will reference both SOM and SoC naming. It is important to understand whether a given document is using pin names/numbers, interface names/instances, and function names/instances with reference to the SOM or to the SoC.

Various documents are provided to help customers design, lay out, build, and configure NVIDIA® Jetson™ module-based designs.

Table 1 lists the main documents that are focused on the hardware or contain references to hardware features.

Table 1. Hardware References and Features Documentation

Document Category	Document Name for Jetson Xavier NX Designs	Description
Data Sheet	Jetson Xavier NX Module Data Sheet	• Module overview • Power and system management • Interface and signal description • Electrical, package, and thermal specifications
Technical Reference Manual (TRM)	Xavier (SoC) Technical Reference Manual	• Address map • Chapters per block (functional description, programming guidelines, and registers)
Product Design Guide	Jetson Xavier NX Product Design Guide	• Power • Interface chapters (connection figures and tables, and routing guidelines)
Carrier Board Specification	Jetson Xavier NX Developer Kit Carrier Board Specification	• Developer Kit features and description • Expansion connector and interface descriptions • Power allocation
Pinmux	Jetson Xavier NX Module Pinmux	• Module pin name and number, SoC ball name

Document Category	Document Name for Jetson Xavier NX Designs	Description
		• SFIO and GPIO options • Wakes, straps POR state
Design files	Jetson Xavier NX Developer Kit Carrier Board Design Files	• Schematics, layout, bill of materials (BOM) • Misc (Assy drawing, stack-up, gerbers, etc)

Pin and Function Names

There are different pin and interface names in many cases on the module vs. chip. Some documents are based on the chip, such as the TRM, while others are based on the module, or may have both chip and module terms and names. This can lead to confusion. It is important to use the right document and to understand whether a term or name is associated with a chip, module pin name or number, an interface name or instance, or a function name or instance.

Pinmux

The Jetson Xavier NX module pinmux (pin multiplexing) spread sheet has the module pin names and pin numbers in the first two columns, and the SoC ball name in the 3rd column. The GPIOs and SFIO functions are covered in the pin muxing area. The portion of the pinmux in Table 2 includes one of the I2S interfaces.

Table 2. Pinmux I2S and MCLK

		MPIO	Pin Muxing				
Signal Name	**Pin #**	**SoC Ball Name**	**GPIO**	**SFIO0**	**SFIO1**	**SFIO2**	**SFIO3**
GPIO09	211	AUD_MCLK	GPIO3_PS.04	AUD_MCLK	–	–	–
I2S1_SCLK	226	DAP3_SCLK	GPIO3_PT.01	I2S3_SCLK	DMIC1_DAT	–	–
I2S1_DOUT	220	DAP3_DOUT	GPIO3_PT.02	I2S3_SDATA_OUT	DMIC1_CLK	–	–
I2S1_DIN	222	DAP3_DIN	GPIO3_PT.03	I2S3_SDATA_IN	DMIC2_DAT	–	–
I2S1_FS	224	DAP3_FS	GPIO3_PT.04	I2S3_LRCK	DMIC2_CLK	–	–

In the case shown in Table 2, for one of the I2S interfaces that are available on the module pins, the following pin/function names exist:

- Module signal names: I2S1_xxx
- SoC chip pin names: DAP3_xxx
- SFIO 0 function names: I2S3_xxx

This shows that the module pin names, chip pin names, and function names can be different. When referring to the various documents, it is important to understand which name form is applicable. For instance, if the TRM is accessed for information on how to configure the pins or functions, it is necessary to know that the TRM is chip focused. It will have SoC pin names when referring to the pins, such as in the "Pinmux Register" section, or function names if the function is being configured. In the case of the module data sheet, the module pin names are relevant. See the following "TRM" and "Data Sheet" sections for details.

Data Sheet

The module data sheet only uses the module pin names. If a programmer needed to know what SoC function to configure, it would be necessary to look at either the pinmux spreadsheet or OEM product design guide to know what SoC function is associated with that module pin.

Table 3. Data Sheet I2S1 and MCLK Pin Descriptions

Pin #	Signal Name	Description	Direction	Pin Type
211	GPIO09	GPIO #9 or Audio Codec Master Clock	Bidir	CMOS – 1.8V
226	I2S1_SCLK	I2S Audio Port 1 Clock	Bidir	CMOS – 1.8V
224	I2S1_FS	I2S Audio Port 1 Left/Right Clock	Bidir	CMOS – 1.8V
220	I2S1_DOUT	I2S Audio Port 1 Data Out	Output	CMOS – 1.8V
222	I2S1_DIN	I2S Audio Port 1 Data In	Input	CMOS – 1.8V

Technical Reference Manual

The technical reference manual (TRM) is based on the chip (for example, Xavier). References to pin names (such as DAP1) will be chip pin names. There are also references to functions (such as I2S1). These should match the names of functions in the pinmux spreadsheet or OEM product design guide. To know what pin on the module an SoC pin is associated with, the pinmux spreadsheet is the best cross reference, although the OEM product design guide has that information as well.

PADCTL_AUDIO_DAP3_FS_0

Offset: 0x48
Read/Write: RW
Parity Protection: N

SCR Protection: SCR_DAP3_FS_0
Reset: 0x00000454 (0bxxxx,xxxx,xxxx,xxxx,xxx0,x1x0,x1x1,0100)

1:0	I2S3	**PM**: **0** = I2S3 **1** = DMIC2 **2** = RSVD2 **3** = RSVD3

Product Design Guide

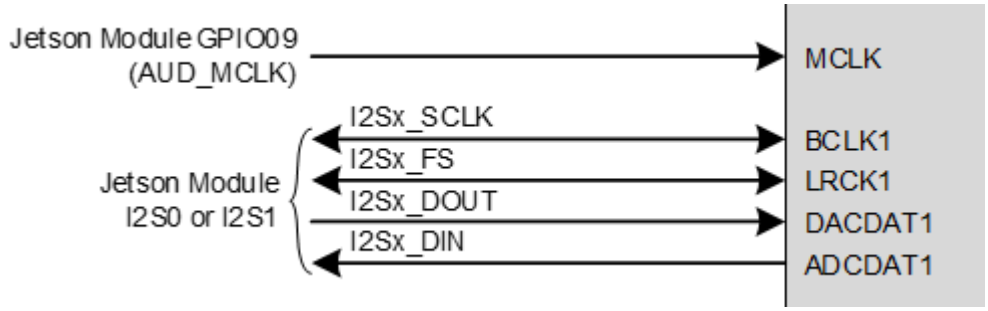
The product design guide focuses on the module, but many of the figures and pin description tables also include the SoC signal associated with a module pin where applicable. The partial table (Table 4) contains the same I2S interface used as the example in the earlier document sections. Both the module (Jetson Xavier NX) and SoC pin names are shown.

Table 4. OEM Design Guide Audio I2S and MCLK Pin Descriptions

Pin #	Module Pin Name	SoC Signal	Usage/Description	Recommended Usage	Direction	Pin Type
211	GPIO09	AUD_MCLK	GPIO #9 or Audio Codec Master Clock	Audio Device	Output	CMOS – 1.8V
226	I2S1_SCLK	DAP3_SCLK	I2S Audio Port 1 Clock	Audio Device (i.e. M.2 Key E)	Bidir	
224	I2S1_FS	DAP3_FS	I2S Audio Port 1 Left/Right Clock		Bidir	
220	I2S1_DOUT	DAP3_DOUT	I2S Audio Port 1 Data Out		Output	
222	I2S1_DIN	DAP3_DIN	I2S Audio Port 1 Data In		Input	

Figure 1 also shows the I2S interface connected to an Audio Codec and includes the module pin names and Codec pin names.

Figure 1. I2S0 or I2S1 Interface Connections to Codec



The following audio connections table contains only the module pin names, or function names in parenthesis if necessary, for clarity.

Table 5. OEM Design Guide Audio I2S and MCLK Signal Connections

Module Pin Name	Type	Termination	Description
I2S[1:0]_SCLK	I/O		I2S Serial Clock: Connect to I2S/PCM CLK pin of audio device.
I2S[1:0]_FS	I/O		I2S Frame Select (Left/Right Clock): Connect to corresponding pin of audio device.
I2S[1:0]_DOUT	I/O		I2S Data Output: Connect to data input pin of audio device.
I2S[1:0]_DIN	I		I2S Data Input: Connect to data output pin of audio device.
GPIO09	O		Audio Codec Master Clock: Connect to clock pin of audio codec.

Developer Kit Carrier Board Specification

The developer kit specification uses module (Jetson Xavier NX) pin names and pin numbers from the carrier board reference design. If it is necessary to know the corresponding SoC name or function, the pinmux should be referenced (the design guide also contains this information).

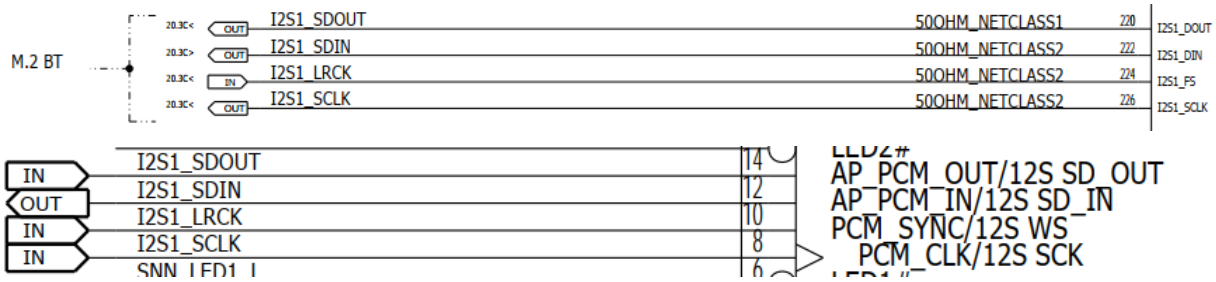
Table 6. I2S Connections to M.2 Key E Socket on Carrier Board

Pin # (M.2)	Module Pin Name	Module Pin #	Usage/Description	Type/Dir
8	I2S1_CLK	226	I2S #1 Clock	Bidir
10	I2S1_FS	224	I2S #1 Left/Right Clock	Bidir
12	I2S1_DIN	222	I2S #1 Data In	Input
14	I2S1_DOUT	220	I2S #1 Data Out	Output

Design Files

The design files (schematics, layout, etc.) also contain only module pin names and net names. Look to the pinmux or OEM design guide if it is necessary to know which chip pin is associated with a module pin name.

Figure 2. Design Schematics



Chip, Module, and Carrier Board Pin Names and Numbers

The information provided in the following table can be found in various hardware documentation (as described within this application note). Table 7 provides a consolidation of this information for your convenience.

Table 7. Chip, Module, and Carrier Board Pinout

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
1	GND	GND	–
2	GND	GND	–
3	CSI1_D0_N	CSI1_D0_N	CSI_B_D0_N
4	CSI0_D0_N	CSI0_D0_N	CSI_A_D0_N
5	CSI1_D0_P	CSI1_D0_P	CSI_B_D0_P
6	CSI0_D0_P	CSI0_D0_P	CSI_A_D0_P
7	GND	GND	–
8	GND	GND	–
9	CSI1_CLK_N	CSI1_CLK_N	CSI_B_CLK_N
10	CSI0_CLK_N	CSI0_CLK_N	CSI_A_CLK_N
11	CSI1_CLK_P	CSI1_CLK_P	CSI_B_CLK_P
12	CSI0_CLK_P	CSI0_CLK_P	CSI_A_CLK_P
13	GND	GND	–
14	GND	GND	–
15	CSI1_D1_N	CSI1_D1_N	CSI_B_D1_N
16	CSI0_D1_N	CSI0_D1_N	CSI_A_D1_N
17	CSI1_D1_P	CSI1_D1_P	CSI_B_D1_P
18	CSI0_D1_P	CSI0_D1_P	CSI_A_D1_P
19	GND	GND	–
20	GND	GND	–
21	CSI3_D0_N	CSI3_D0_N	CSI_D_D0_N

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
22	CSI2_D0_N	CSI2_D0_N	CSI_C_D0_N
23	CSI3_D0_P	CSI3_D0_P	CSI_D_D0_P
24	CSI2_D0_P	CSI2_D0_P	CSI_C_D0_P
25	GND	GND	–
26	GND	GND	–
27	CSI3_CLK_N	CSI3_CLK_N	CSI_D_CLK_N
28	CSI2_CLK_N	CSI2_CLK_N	CSI_C_CLK_N
29	CSI3_CLK_P	CSI3_CLK_P	CSI_D_CLK_P
30	CSI2_CLK_P	CSI2_CLK_P	CSI_C_CLK_P
31	GND	GND	–
32	GND	GND	–
33	CSI3_D1_N	CSI3_D1_N	CSI_D_D1_N
34	CSI2_D1_N	CSI2_D1_N	CSI_C_D1_N
35	CSI3_D1_P	CSI3_D1_P	CSI_D_D1_P
36	CSI2_D1_P	CSI2_D1_P	CSI_C_D1_P
37	GND	GND	–
38	GND	GND	–
39	DP0_TXD0_N	DP0_TXD0_N	HDMI_DP0_TXD0_N
40	CSI4_D2_N	CSI4_D2_N	CSI_F_D0_N
41	DP0_TXD0_P	DP0_TXD0_P	HDMI_DP0_TXD0_P
42	CSI4_D2_P	CSI4_D2_P	CSI_F_D0_P
43	GND	GND	–
44	GND	GND	–
45	DP0_TXD1_N	DP0_TXD1_N	HDMI_DP0_TXD1_N
46	CSI4_D0_N	CSI4_D0_N	CSI_E_D0_N
47	DP0_TXD1_P	DP0_TXD1_P	HDMI_DP0_TXD1_P
48	CSI4_D0_P	CSI4_D0_P	CSI_E_D0_P
49	GND	GND	–
50	GND	GND	–
51	DP0_TXD2_N	DP0_TXD2_N	HDMI_DP0_TXD2_N
52	CSI4_CLK_N	CSI4_CLK_N	CSI_E_CLK_N
53	DP0_TXD2_P	DP0_TXD2_P	HDMI_DP0_TXD2_P
54	CSI4_CLK_P	CSI4_CLK_P	CSI_E_CLK_P
55	GND	GND	–
56	GND	GND	–
57	DP0_TXD3_N	DP0_TXD3_N	HDMI_DP0_TXD3_N
58	CSI4_D1_N	CSI4_D1_N	CSI_E_D1_N

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
59	DP0_TXD3_P	DP0_TXD3_P	HDMI_DP0_TXD3_P
60	CSI4_D1_P	CSI4_D1_P	CSI_E_D1_P
61	GND	GND	–
62	GND	GND	–
63	DP1_TXD0_N	HDMI_TX2_N	HDMI_DP1_TXD0_N
64	CSI4_D3_N	CSI4_D3_N	CSI_F_D1_N
65	DP1_TXD0_P	HDMI_TX2_P	HDMI_DP1_TXD0_P
66	CSI4_D3_P	CSI4_D3_P	CSI_F_D1_P
67	GND	GND	–
68	GND	GND	–
69	DP1_TXD1_N	HDMI_TX1_N	HDMI_DP1_TXD1_N
70	DSI_D0_N	CSI5_D0_N	CSI_G_D0_N
71	DP1_TXD1_P	HDMI_TX1_P	HDMI_DP1_TXD1_P
72	DSI_D0_P	CSI5_D0_P	CSI_G_D0_P
73	GND	GND	–
74	GND	GND	–
75	DP1_TXD2_N	HDMI_TX0_N	HDMI_DP1_TXD2_N
76	DSI_CLK_N	CSI5_CLK_N	CSI_G_CLK_N
77	DP1_TXD2_P	HDMI_TX0_P	HDMI_DP1_TXD2_P
78	DSI_CLK_P	CSI5_CLK_P	CSI_G_CLK_P
79	GND	GND	–
80	GND	GND	–
81	DP1_TXD3_N	HDMI_TXC_N	HDMI_DP1_TXD3_N
82	DSI_D1_N	CSI5_D1_N	CSI_G_D1_N
83	DP1_TXD3_P	HDMI_TXC_P	HDMI_DP1_TXD3_P
84	DSI_D1_P	CSI5_D1_P	CSI_G_D1_P
85	GND	GND	–
86	GND	GND	–
87	GPIO00	USB0_VBUS_DET*	USB_VBUS_EN0
88	DP0_HPD	DP0_HPD	DP_AUX_CH0_HPD
89	SPI0_MOSI	SPI0_MOSI	SPI1_MOSI
90	DP0_AUX_N	DP0_AUX_N	DP_AUX_CH0_N
91	SPI0_SCK	SPI0_SCK	SPI1_SCK
92	DP0_AUX_P	DP0_AUX_P	DP_AUX_CH0_P
93	SPI0_MISO	SPI0_MISO	SPI1_MISO
94	HDMI_CEC	HDMI_CEC	HDMI_CEC
95	SPI0_CS0*	SPI0_CS0	SPI1_CS0

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
96	DP1_HPD	HDMI_HPD	DP_AUX_CH1_HPD
97	SPI0_CS1*	SPI0_CS1	SPI1_CS1
98	DP1_AUX_N	HDMI_DDC_SDA	DP_AUX_CH1_N
99	UART0_TXD	UART0_TXD	UART2_TX
100	DP1_AUX_P	HDMI_DDC_SCL	DP_AUX_CH1_P
101	UART0_RXD	UART0_RXD	UART2_RX
102	GND	GND	–
103	UART0_RTS*	UART0_RTS	UART2_RTS
104	SPI1_MOSI	SPI1_MOSI	SPI3_MOSI
105	UART0_CTS*	UART0_CTS	UART2_CTS
106	SPI1_SCK	SPI1_SCK	SPI3_SCK
107	GND	GND	–
108	SPI1_MISO	SPI1_MISO	SPI3_MISO
109	USB0_D_N	USB0_AP_N	USB0_DN
110	SPI1_CS0*	SPI1_CS0	SPI3_CS0
111	USB0_D_P	USB0_AP_P	USB0_DP
112	SPI1_CS1*	SPI1_CS1	SPI3_CS1
113	GND	GND	–
114	CAM0_PWDN	CAM0_PWDN	SOC_GPIO04
115	USB1_D_N	USB1_AP_N	USB1_DN
116	CAM0_MCLK	CAM0_MCLK	EXTPERIPH1_CLK
117	USB1_D_P	USB1_AP_P	USB1_DP
118	GPIO01	GPIO01	SOC_GPIO41
119	GND	GND	–
120	CAM1_PWDN	CAM1_PWDN	SOC_GPIO05
121	USB2_D_N	USB2_AP_N	USB2_DN
122	CAM1_MCLK	CAM1_MCLK	EXTPERIPH2_CLK
123	USB2_D_P	USB2_AP_P	USB2_DP
124	GPIO02	BT_M2_WAKE_AP	SOC_GPIO23
125	GND	GND	–
126	GPIO03	BT_M2_EN	SPI2_SCK
127	GPIO04	PWR_LED_CTRL	SPI2_MISO
128	GPIO05	W_DISABLE1_CTRL	SPI2_MOSI
129	GND	GND	–
130	GPIO06	CAM_MUX_SEL	SPI2_CS0_N
131	PCIE0_RX0_N	PCIE0_RX0_N	NVHS0_RX0_N
132	GND	GND	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
133	PCIE0_RX0_P	PCIE0_RX0_P	NVHS0_RX0_P
134	PCIE0_TX0_N	PCIE0_TX0_N	NVHS0_TX0_N
135	GND	GND	–
136	PCIE0_TX0_P	PCIE0_TX0_P	NVHS0_TX0_P
137	PCIE0_RX1_N	PCIE0_RX1_N	NVHS0_RX1_N
138	GND	GND	–
139	PCIE0_RX1_P	PCIE0_RX1_P	NVHS0_RX1_P
140	PCIE0_TX1_N	PCIE0_TX1_N	NVHS0_TX1_N
141	GND	GND	–
142	PCIE0_TX1_P	PCIE0_TX1_P	NVHS0_TX1_P
143	CAN_RX	CAN_RX	CAN0_DIN
144	GND	GND	–
145	CAN_TX	CAN_TX	CAN0_DOUT
146	GND	GND	–
147	GND	GND	–
148	PCIE0_TX2_N	PCIE0_TX2_N	NVHS0_TX2_N
149	PCIE0_RX2_N	PCIE0_RX2_N	NVHS0_RX2_N
150	PCIE0_TX2_P	PCIE0_TX2_P	NVHS0_TX2_P
151	PCIE0_RX2_P	PCIE0_RX2_P	NVHS0_RX2_P
152	GND	GND	–
153	GND	GND	–
154	PCIE0_TX3_N	PCIE0_TX3_N	NVHS0_TX3_N
155	PCIE0_RX3_N	PCIE0_RX3_N	NVHS0_RX3_N
156	PCIE0_TX3_P	PCIE0_TX3_P	NVHS0_TX3_P
157	PCIE0_RX3_P	PCIE0_RX3_P	NVHS0_RX3_P
158	GND	GND	–
159	GND	GND	–
160	PCIE0_CLK_N	PCIE0_CLK_N	PEX_CLK5N or NVHS0_REFCLK_N
161	USBSS_RX_N	USBSS_TX_HUB_N	UPHY_RX1_N
162	PCIE0_CLK_P	PCIE0_CLK_P	PEX_CLK5P or NVHS0_REFCLK_P
163	USBSS_RX_P	USBSS_TX_HUB_P	UPHY_RX1_P
164	GND	GND	–
165	GND	GND	–
166	USBSS_TX_N	USBSS_TX_N	UPHY_TX1_N
167	PCIE1_RX0_N	PCIE1_RX0_N	UPHY_RX0_N

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
168	USBSS_TX_P	USBSS_TX_P	UPHY_TX1_P
169	PCIE1_RX0_P	PCIE1_RX0_P	UPHY_RX0_P
170	GND	GND	–
171	GND	GND	–
172	PCIE1_TX0_N	PCIE1_TX0_N	UPHY_TX0_N
173	PCIE1_CLK_N	PCIE1_CLK_N	PEX_CLK1_N
174	PCIE1_TX0_P	PCIE1_TX0_P	UPHY_TX0_P
175	PCIE1_CLK_P	PCIE1_CLK_P	PEX_CLK1_P
176	GND	GND	–
177	GND	GND	–
178	MOD_SLEEP*	MOD_SLEEP*	SOC_PWR_REQ
179	PCIE_WAKE*	PCIE_WAKE	PEX_WAKE_N
180	PCIE0_CLKREQ*	PCIE0_CLKREQ	PEX_L5_CLKREQ_N
181	PCIE0_RST*	PCIE0_RST	PEX_L5_RST_N
182	PCIE1_CLKREQ_N	PCIE1_CLKREQ	PEX_L1_CLKREQ_N
183	PCIE1_RST_N	PCIE1_RST	PEX_L1_RST_N
184	GBE_MDI0_N	GBE_MDI0_N	–
185	I2C0_SCL	ID_I2C_SCL	GEN2_I2C_SCL
186	GBE_MDI0_P	GBE_MDI0_P	–
187	I2C0_SDA	ID_I2C_SDA	GEN2_I2C_SDA
188	GBE_LED_LINK	GBE_LED_LINK	–
189	I2C1_SCL	I2C1_SCL	DP_AUX_CH3_P
190	GBE_MDI1_N	GBE_MDI1_N	–
191	I2C1_SDA	I2C1_SDA	DP_AUX_CH3_N
192	GBE_MDI1_P	GBE_MDI1_P	–
193	I2S0_DOUT	I2S0_SDOUT	DAP5_DOUT
194	GBE_LED_ACT	GBE_LED_ACT	–
195	I2S0_DIN	I2S0_SDIN	DAP5_DIN
196	GBE_MDI2_N	GBE_MDI2_N	–
197	I2S0_FS	I2S0_LRCK	DAP5_FS
198	GBE_MDI2_P	GBE_MDI2_P	–
199	I2S0_SCLK	I2S0_SCLK	DAP5_SCLK
200	GND	GND	–
201	GND	GND	–
202	GBE_MDI3_N	GBE_MDI3_N	–
203	UART1_TXD	UART1_TXD	UART1_TX
204	GBE_MDI3_P	GBE_MDI3_P	–

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
205	UART1_RXD	UART1_RXD	UART1_RX
206	GPIO07	GPIO07	SOC_GPIO44
207	UART1_RTS*	UART1_RTS	UART1_RTS
208	GPIO08	FAN_TACH	SOC_GPIO22
209	UART1_CTS*	UART1_CTS	UART1_CTS
210	CLK_32K_OUT	SUSCLK_32KHZ	(PMIC GPIO4 32K CLK Out)
211	GPIO09	GPIO09	AUD_MCLK
212	GPIO10	M2E_ALERT*	SOC_GPIO21
213	CAM_I2C_SCL	CAM_I2C_SCL	CAM_I2C_SCL
214	FORCE_RECOVERY*	FORCE_RECOVERY*	FORCE_RECOVERY_N
215	CAM_I2C_SDA	CAM_I2C_SDA	CAM_I2C_SDA
216	GPIO11	GPIO11	SOC_GPIO42
217	GND	GND	–
218	GPIO12	GPIO12	TOUCH_CLK
219	SDMMC_DAT0	SDIO_D0	SDMMC3_DAT0
220	I2S1_DOUT	I2S1_SDOUT	DAP3_DOUT
221	SDMMC_DAT1	SDIO_D1	SDMMC3_DAT1
222	I2S1_DIN	I2S1_SDIN	DAP3_DIN
223	SDMMC_DAT2	SDIO_D2	SDMMC3_DAT2
224	I2S1_FS	I2S1_LRCK	DAP3_FS
225	SDMMC_DAT3	SDIO_D3	SDMMC3_DAT3
226	I2S1_SCLK	I2S1_SCLK	DAP3_SCLK
227	SDMMC_CMD	SDIO_CMD	SDMMC3_CMD
228	GPIO13	GPIO13	SOC_GPIO54
229	SDMMC_CLK	SDIO_CLK	SDMMC3_CLK
230	GPIO14	FAN_PWM	SOC_GPIO12
231	GND	GND	–
232	I2C2_SCL	I2C2_SCL	GEN1_I2C_SCL
233	SHUTDOWN_REQ*	SHUTDOWN_REQ*	–
234	I2C2_SDA	I2C2_SDA	GEN1_I2C_SDA
235	PMIC_BBAT	BBAT	(PMIC BBATT)
236	UART2_TXD	UART2_TXD	UART3_TX
237	POWER_EN	POWER_EN	(PMIC EN0 through converter logic)
238	UART2_RXD	UART2_RXD	UART1_RX
239	SYS_RESET*	SYS_RST*	SYS_RESET_IN_N
240	SLEEP/WAKE*	PWR_BTN*	POWER_ON

Conn. Pin #	Carrier Board Symbol Pin Name	Carrier Board Net Name	SoC Pin Name
241	GND	GND	–
242	GND	GND	–
243	GND	GND	–
244	GND	GND	–
245	GND	GND	–
246	GND	GND	–
247	GND	GND	–
248	GND	GND	–
249	GND	GND	–
250	GND	GND	–
251	VDD_IN	VDD_5V_SYS	–
252	VDD_IN	VDD_5V_SYS	–
253	VDD_IN	VDD_5V_SYS	–
254	VDD_IN	VDD_5V_SYS	–
255	VDD_IN	VDD_5V_SYS	–
256	VDD_IN	VDD_5V_SYS	–
257	VDD_IN	VDD_5V_SYS	–
258	VDD_IN	VDD_5V_SYS	–
259	VDD_IN	VDD_5V_SYS	–
260	VDD_IN	VDD_5V_SYS	–

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